Toward A Fully Integrated Neurostimulator With Inductive Power Recovery Front-End

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***Abstract*—In order to investigate new neurostimulation strategies for micturition recovery in spinal cord injured patients, custom implantable stimulators are required to carry-on chronic animal experiments. However, higher integration of the neurostimulator becomes increasingly necessary for miniaturization purposes, power consumption reduction, and for increasing the number of stimulation channels. As a first step towards total integration, we present in this paper the design of a highly-integrated neurostimulator that can be assembled on a 21-mm diameter printed circuit board. The prototype is based on three custom integrated circuits fabricated in High-Voltage (HV) CMOS technology, and a low-power small-scale commercially available FPGA. Using a step-down approach where the inductive voltage is left free up to 20 V, the inductive power and data recovery front-end is fully integrated. In particular, the front-end includes a bridge rectifier, a 20-V voltage limiter, an adjustable series regulator (5 to 12 V), a switched-capacitor step-down DC/DC converter (1:3, 1:2, or 2:3 ratio), as well as data recovery. Measurements show that the DC/DC converter achieves more than 86% power efficiency while providing around 3.9-V from a 12-V input at 1-mA load, 1:3 conversion ratio, and 50-kHz switching frequency. With such efficiency, the proposed step-down inductive power recovery topology is more advantageous than its conventional step-up counterpart. Experimental results confirm good overall functionality of the system.**

***Index Terms*—Complementary metal-oxide semiconductor (CMOS) integrated circuits, data demodulation and decoding, high-voltage techniques, implantable biomedical devices, inductive power transmission, rectifiers, switched-capacitor DC-DC converters, voltage limiters.**

I. Introduction

FUNCTIONAL ELECTRICAL STIMULATION (FES) has been investigated at different sites of the human body in order to restore organs or limbs function in spinal cord injured (SCI) patients for example. Sacral neurostimulation to recover the voluntary control of micturition is one of the most challenging FES applications. The efficiency of neurostimulation in this case depends on the capability to contract selectively the bladder muscle (detrusor) without triggering contraction of the external urethral sphincter (EUS) muscle, while both share the same sacral nerves as common innervations pathways. In case of a complete SCI, dorsal rhizotomy—which consists of selectively severing afferent sacral nerve roots that are involved in pathological reflex arc—is combined with an implantable sacral ventral root stimulator such as the Finetech-Brindley Bladder System (VOCARE) [1]. In fact, this neurostimulation system is the only commercialized and FDA-approved solution aiming for micturition in SCI patients [2]. Unfortunately, rhizotomy being irreversible, it has a fundamental disadvantage which is the abolition of sexual and defecation reflexes, as well as sacral sensations if still present in case of incomplete SCI. Polystim Lab. recently proposed a new multi-site sacral neurostimulation strategy to enhance micturition, based on nerve conduction blockade using high frequency stimulation as an alternative to rhizotomy. Preliminary results obtained with this strategy in acute dog experiments were presented [3]. However, such experiments are not sufficient to validate the strategy especially that spinal shock generally lasts several weeks after SCI. Chronic experiments are mandatory in order to evaluate the long-term efficiency. This obviously requires a custom implantable neurostimulator that implements the proposed strategy, and will be capable of simultaneously generating conventional stimulation waveforms as well as high-frequency sinewaves over multiple channels. A preliminary version of this neurostimulator has been designed using commercially available discrete components [4]. The inductive power and data recovery front-end (Fig. 1) of this neurostimulator will be briefly described. Then, the design of a highly-integrated neurostimulator that is based on three custom integrated circuits (IC1 to 3) will be elaborated. ICs have been fabricated in DALSA Semiconductor High-Voltage (HV) 20 V CMOS technology (C08E). While IC3 includes a stimulation stage previously reported [5], IC1 and IC2 form a complete new HV RF front-end that will be elaborated in this paper with a focus on voltage rectification, limitation, and step-down DC/DC conversion, as well as data recovery.

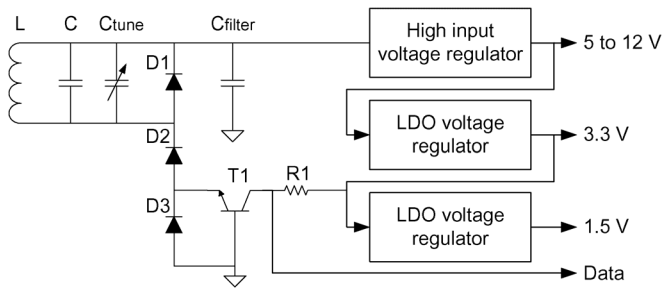

Fig. 1. Power and data recovery front-end in discrete components based neurostimulator.

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II. Discrete Components Based Neurostimulator

In order to transmit energy and data wirelessly to the implanted neurostimulator, near-field inductive coupling with an external controller is used. The inductive power and data recovery front-end, as implemented in the previous neurostimulator, is presented in Fig. 1. Inductive power is recovered by the parallel LC network resonating at the field frequency. Electromagnetic energy penetrates skin tissues with minimum losses between 1 and 10 MHz. Higher frequencies are prone to tissues absorption and lower frequencies to skin-air interface reflection. However, taking into account coupling attenuation through skin tissues and inductors characteristics while complying with the Industrial, Scientific and Medical (ISM) radio band, the chosen inductive coupling frequency is 13.56 MHz [26]. Inductor L is custom-made using a thin and flexible printed circuit board (PCB). It is a 3-turn spiral antenna with 38-mm external diameter and 1-mm trace width to reduce its series resistance. Capacitor C is a set of HV parallel ceramic capacitors with high quality factor and stable characteristics under varying voltage and temperature. To recover maximum inductive energy, the LC resonant frequency must be tuned. This is achieved manually before packaging thanks to the miniature variable capacitor Ctune. With optimum tuning, high inductive coupling, and weak load conditions, the alternating signal across the LC network can exceed 60-V peak-to-peak amplitude in our system. This signal is rectified by the voltage-doubler consisting of diodes (D1, D2), then filtered by a large capacitor Cfilter (6.8 μF/50 V) which acts as an energy storage for the implanted stimulator. From the resulting filtered but still unregulated high voltage, three linear regulators connected in series provide different supply voltages to the stimulator system. 1.5 V supply is used for the core of the control unit, a Field Programmable Gate Array (FPGA). 3.3 V supply is used for the FPGA's I/O buffers, digital to analog converters (DAC), and logic supply of CMOS switches in stimulation and monitoring stages. Finally, adjustable 5 to 12 V supply is used for current sources and analog supply of CMOS switches in stimulation and monitoring stages. Because the high input voltage regulator can operate up to 80 V, voltage limiting of the rectified signal is not needed as it is indirectly limited by the maximum available inductive power and the minimum system power consumption. This approach allows recovering 5 to 12 V supply for stimulation without using a step-up DC/DC converter as in topologies where the inductive voltage is limited to lower values. For data transmission, On-Off Keying (OOK) modulation scheme is used because of the design simplicity of demodulation which can be implemented as a simple lower-envelope detector. Indeed, by adding diode D3 in series between the rectifier and the ground, small variations due to the carrier modulation can be detected and amplified by common-base transistor T1 and pull-up resistor R1.

III. Highly-Integrated Neurostimulator

A. Architecture

The design of implantable prototypes using commercially available discrete components allowed testing previous stimulation strategies in chronic dog experiments. For the proposed new FES strategy there are three main constraints on the neurostimulator design: 1) at least 4 channels to stimulate different sacral nerves with optimized parameters, 2) smaller animals for chronic experiments, and 3) recovered inductive power limited to 50 mW. Thus, custom and higher integration of the neurostimulator becomes increasingly necessary for larger number of channels, miniaturization and power consumption reduction. Previous integration work covered stimulation and monitoring stages [5], [6], eventually integrating the control unit [7]. However, the inductive power and data recovery front-end remained the most difficult to fully integrate, especially because of the rectifier stage and the high voltages involved in near-field inductive coupling. So, as a first step towards full integration, the proposed highly-integrated neurostimulator is illustrated in Fig. 2. It is based on custom integrated circuits IC1 to 3 (Figs. 3–5 respectively), fabricated in HV (20 V) CMOS DALSA semiconductor C08E technology. IC1 and IC2 integrate the inductive power recovery front-end using a new step-down topology [8], [9]. They include HV signal rectification, regulation and DC-DC conversion as well as data recovery. IC3 integrates a HV single-output stimulation stage that includes an 8-bit current mode DAC based on a modified thermometer decoder architecture which minimizes the required HV transistors [5]. The neurostimulator offers 4 bipolar

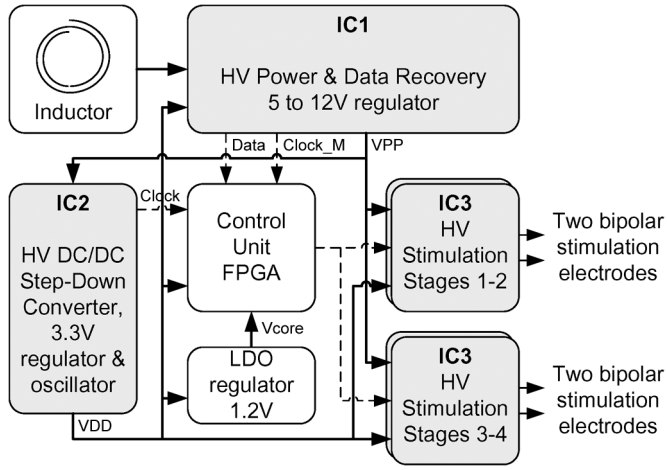

Fig. 2. Architecture of the highly-integrated neurostimulator.

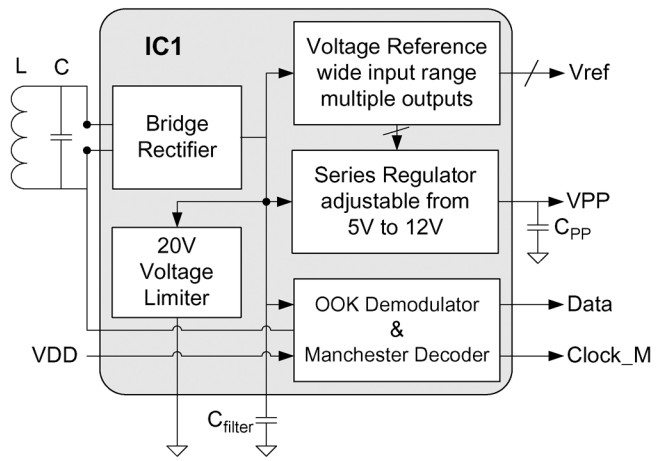

Fig. 3. Block diagram of IC1.

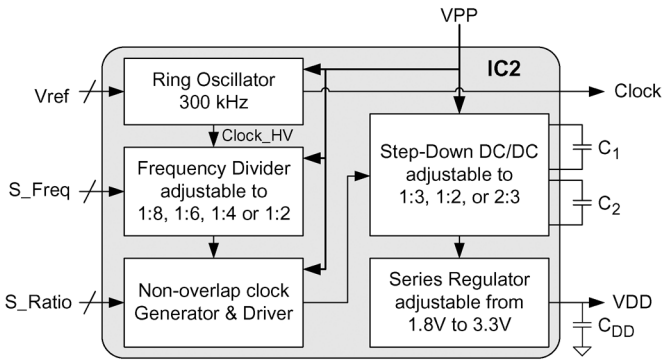

Fig. 4. Block diagram of IC2.

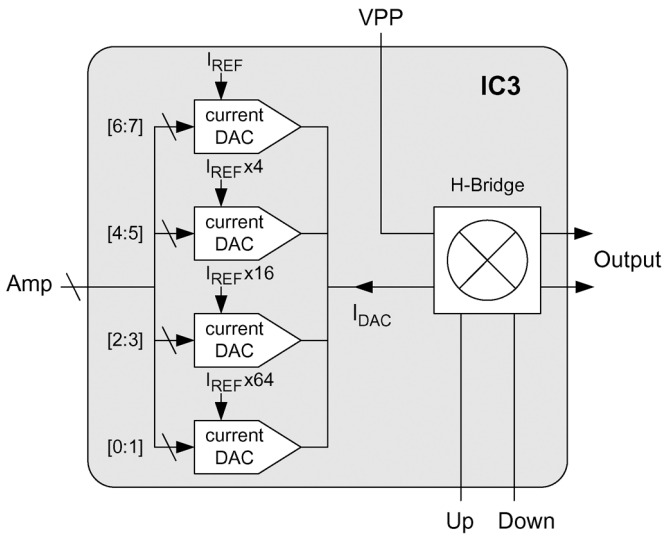

Fig. 5. Block diagram of IC3.

outputs using IC3 four times. The control unit could have been integrated as well, but it is not necessarily advantageous at this early stage as its code is continuously being improved and adapted. Instead, one of the latest generations of FPGA (Igloo, ACTEL) is used to benefit from several advantages such as low-power, small-scale package, and especially In-Sytem Programming (ISP) feature. The latter would allow wired re-programming of the FPGA after assembly of the system or even after packaging if needed. This FPGA is similar to that chosen for the discrete components based neurostimulator but, to reduce power consumption even more, its core runs at a lower voltage supply of 1.2 V that requires an additional low dropout (LDO) regulator. At 300-kHz clock frequency, the FPGA core current consumption is less than 100 μA which is around 10 times less than previous nonreprogrammable FPGA (Ex, ACTEL).

B. Integrated Power and Data Recovery

In most inductively-powered systems, minimizing the inductive voltage is preferred in general as it would improve the inductive link power efficiency. In sacral neurostimulation however, the high electrode-nerve interface impedance leads to a dual-supply requirement where high voltage supply is mandatory for high current stimulation and low voltage supply is needed to reduce power consumption of digital processing and most analog components. A conventional solution is to limit the inductive voltage to a low value and to use a step-up DC/DC converter to generate a HV supply [5], [13]. Limiting the voltage is required to protect the system from inductive voltages that may largely exceed the compliance of low-voltage ICs in certain conditions. This can be achieved by providing a low impedance path to ground. Voltage can be limited off-chip using Zener diodes or shunt regulators but also on-chip using different voltage clamp techniques with diodes or controlled transistors as shunting devices [10]–[16]. Nevertheless, the inductive power needed for high current stimulation pulses becomes an excess of power in periods of time where stimulation is off. This excess of inductive power when not used by the system leads to an excess of current that is simply dissipated by the voltage limiter in the form of heat. In addition, according to the theoretical study published in [17], the step-up approach is not necessarily the most advantageous topology when considering total efficiency of the system and taking into account the load current on each supply, the inductive-link secondary equivalent source resistance, and the converter efficiency. In fact, considering actual parameters of this neurostimulation system (above 1 mA current consumption from 3.3 V supply, 2 mA stimulation pulses from 10 V supply, around 12 kΩ equivalent source resistance) and the output impedance of DC/DC converters that is generally of the order of 100 Ω, a step-down approach would be more efficient if the converter efficiency is higher than 40% [9]. Moreover, using a HV technology it is possible not to limit the inductive voltage as in the discrete components based neurostimulator. The advantage then would be that the excess of inductive power can be translated to charge that can be stored in the filtering capacitor, instead of being heat-dissipated. Thus, the implementation of the inductive power and data recovery front-end in HV CMOS technology is proposed using a step-down approach where the inductive voltage is left free (up to 20 V for C08E technology) as shown in Figs. 3 and 4. IC1 includes a bridge rectifier, a 20 V voltage limiter, a wide input range voltage reference with multiple outputs, a series regulator delivering an output (VPP) that can be adjusted from 5 to 12 V, as well as an OOK demodulator and a Manchester decoder for data recovery. This design is an advanced version of the one presented in [8]. IC2 includes a switched-capacitor (SC) step-down DC/DC converter whose conversion ratio can be programmed to 1:3, 1:2, or 2:3. The SC converter is driven by full-rail swing nonoverlapping clock phases at a programmable frequency of 37.5, 50, 75 or 150 kHz. Given the low switching frequency, capacitors C1 and C2 are external. After the SC converter, another series regulator provides a supply voltage (VDD) that can be adjusted from 1.8 to 3.3 V. In previous discrete components based neurostimulators built in our laboratory [4], the clock recovered from the Manchester-coded data (Clock_M) was used as a time base for stimuli generation. However, Clock_M suffers from time jitter due to inductive noise during data demodulation. Timing being very important for biphasic stimulation for example where positive and negative phases must have the exact same duration so that total charge injection is null, a much less noisy clock is required. The ring oscillator used to drive the SC

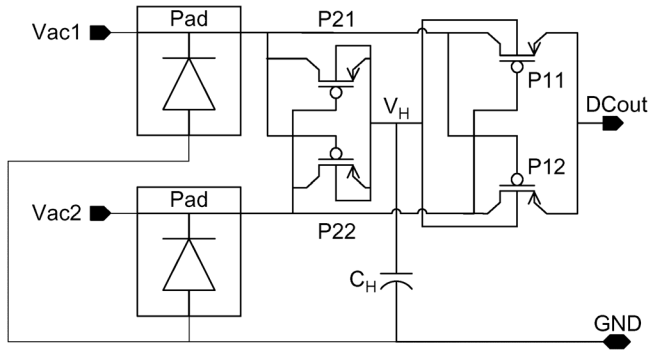

Fig. 6. Schematic of the HV bridge rectifier in IC1.

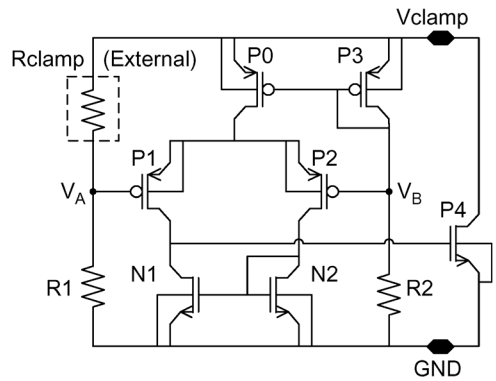

Fig. 7. Schematic of the voltage limiter.

converter brings a simple low power solution to this problem and provides a 300 kHz reference "Clock" for the FPGA and for stimuli generation.

C. Bridge Rectifier

In previous work, we implemented and compared two high-voltage rectifier designs, a voltage-doubler and a bridge rectifier [8]. They were optimized with post-layout simulations to achieve more than 90% power efficiency at 1-mA load and provide enough room for 12-V regulation at 3-mA load and a maximum available inductive power of 50 mW only. Still, the bridge rectifier seemed more advantageous as it provided a higher output voltage (for the same input power) and better power efficiency at higher loads, presented 3 to 4 times higher equivalent input impedance, and required only about half silicon area compared to the voltage-doubler. Both rectifier designs included substrate leakage current and latch-up protections. Unfortunately, even if simulation results were promising, measurements showed high input current draw and latch-up for higher load currents and higher input voltages. In the process of investigating these issues, we found that a specific Laterally Diffused MOS transistor (LDMOS) that has been used in both rectifiers and in other building blocks (data demodulation) as well was not suitable. It has been chosen for its lower ON resistance (Ron) for a relatively smaller area, but its model was considered preliminary in the C08E design kit when we used it. However, this may not be the only explanation for substrate leakage currents and latch-up. Thus, we implemented the rectifier shown in Fig. 6. It is a bridge rectifier formed by cross-coupled PMOS transistors (P11 and P12), and NMOS diodes included in pads with ESD protection with respect to GND. In all schematics HV transistor symbols of the C08E design kit are adopted. All used HV transistors are bidirectional devices with double extended channels and around 1 V threshold voltage. They can operate at gate-source (Vgs) and drain-source (Vds) voltages up to 20 V with breakdown voltage above 30 V. Both PMOS and NMOS devices can have a floating source up to 20 V relative to their bulk. The PMOS device models are fully scalable but the provided NMOS models are limited to either a fixed gate length or a fixed width. Cross-coupling allows achieving low Ron by using opposite-phase signals to switch-on harder much smaller transistors [18], [25]. The cross-coupled transistors P21 and P22 form a dummy half-bridge, which being loaded by a filtering capacitor C_H only, provides the highest possible voltage (V_H) from Vac1 and Vac2. The V_H voltage is applied to the bulk of all PMOS transistors to protect them from latch-up in high load conditions. This PMOS half-bridge structure (P11, P12, P21, P22, C_H) is identical to our previous design. Not including the remaining NMOS half-bridge structure (which contained the LDMOS transistor) and using instead ESD protection diodes as part of the rectifier, was initially part of the investigation to confirm if the implemented PMOS half-bridge structure is not also prone to substrate leakage currents and latch-up. However, the resulting rectifier shows similar post-layout simulation results and can potentially become an interesting approach to save even more silicon area and to decrease chances of latch-up occurrence.

D. Voltage Limiter

In the proposed inductive power recovery step-down approach, the rectified voltage is indirectly limited by the maximum inductive power and the minimum system power consumption. No voltage limiting would be needed with a HV CMOS technology that can withstand the maximum inductive voltage. DALSA semiconductor C08G that can operate up to 300-V (Vds), was considered initially but was ruled out because of the 5-V (Vgs) limitation that makes the design of several building blocks complicated if not unfeasible. With the C08E technology, the rectified voltage must be limited to 20 V. Fig. 7 presents the schematic of the voltage limiter that has been implemented for that purpose. While V_A node is directly proportional to Vclamp through the voltage divider (R1, Rclamp), V_B node follows Vclamp minus one Vgs set by the diode-connected transistor P3 and large biasing resistor R2. The PMOS differential pair (P1, P2) compares both nodes and when V_B becomes higher than V_A, the gate of transistor P4 is pulled-up. This sets a clamp threshold beyond which transistor P4 is turned-on, short-cutting Vclamp to ground until (assuming a limited available input power) it eventually gets lower than the threshold. The clamp threshold can be adjusted with the external resistor Rclamp. Fig. 8 shows a simulation of the voltage limiter I/V characteristic at different clamp thresholds. With 50-mW available power and 800-kΩ Rclamp

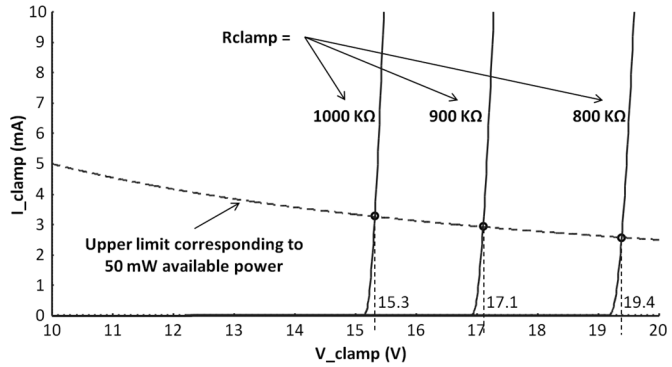

Fig. 8. Simulation of the voltage limiter I/V characteristic at different clamp thresholds.

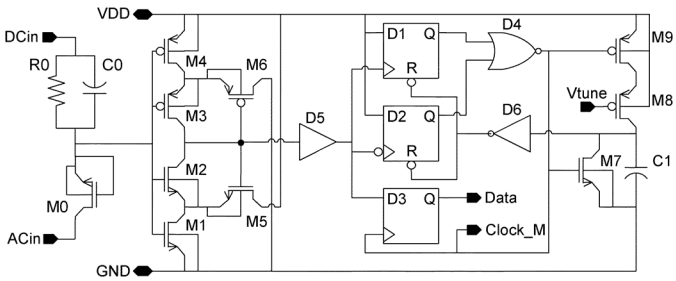

Fig. 9. Schematic of the OOK demodulator and Manchester decoder.

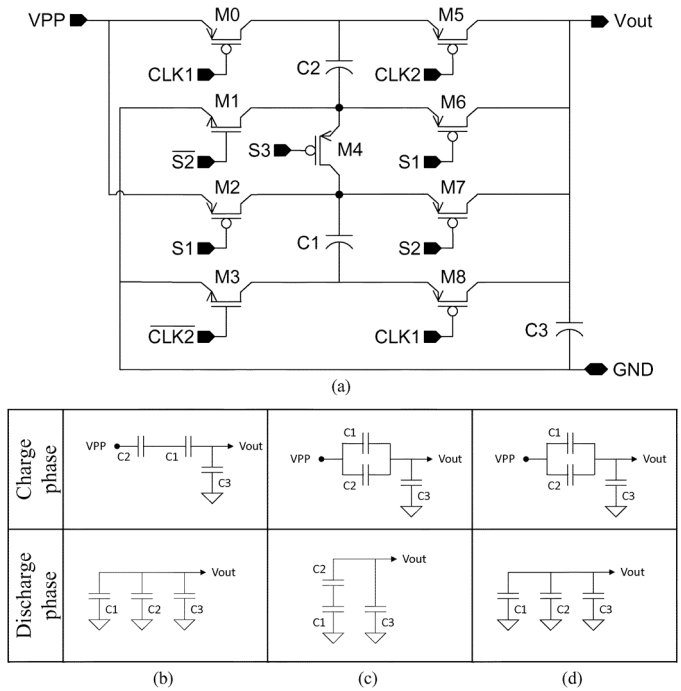

Fig. 10. The DC/DC converter core (a) schematic and its configuration at charging ($\mathrm{CLK1} = \mathrm{GND}, \mathrm{CLK2} = \mathrm{VPP}$) and discharging ($\mathrm{CLK1} = \mathrm{VPP}$, $\mathrm{CLK2} = \mathrm{GND}$) phases for step-down ratios of (b) 1/3, (c) 2/3, and (d) 1/2.

for example, Vclamp will be limited to 19.4 V and the voltage limiter will pass around 2.6 mA.

E. Data Recovery

The schematic of the demodulator and decoder is given in Fig. 9. The OOK demodulator consists of an envelope detector and a Schmitt trigger, where only HV transistors are used. The envelope detector is formed by the diode-connected transistor M0 and the parallel filter (R0//C0) that is adjusted to follow the lower envelope of the inductive voltage ACin. That envelope corresponds to the OOK modulation at 600 kHz. However, the carrier frequency is not completely filtered and a Schmitt trigger inverter (M1–M6) with its different rising and falling thresholds is required to provide a digital signal that is not affected by the carrier transitions. The Schmitt trigger output is a Manchester coded signal that goes through multiple-stage buffer (D5) to obtain steep transitions for better decoding. The Manchester decoder consists of a transition detection circuit formed by the D flip-flops (D1, D2) that drive the NOR gate (D4). At a transition of the Manchester coded signal, the NOR gate output (Clock_M signal) gets low, transistor M9 is switched ON, M7 is switched OFF, and capacitor C1 gets charged through the MOS resistance M8. The charging rate can be adjusted with the M8 gate voltage Vtune. When the voltage across C1 reaches the inverter D6 threshold, D1 and D2 are reset, the signal Clock_M gets high, and C1 gets immediately discharged by M7. It is at the Clock_M rising edge that the Manchester coded signal is sampled by D3 flip-flop. The C1 charging rate is adjusted so that the clock duty cycle is around 3/4 of the Manchester-coded signal. Note that transistors M7–M9 and logic circuits D1-D6 are 5 V CMOS devices.

F. High-Voltage Step-Down DC/DC Converter

Considering the neurostimulator requirements, the switched-capacitor (SC) topology is particularly well suited. An inductor-based buck converter may provide higher efficiency but it remains a costly, bulky and noisy solution that is usually dedicated for much higher loads [19]. Still, many step-down SC converter designs with a variety of regulation control schemes were reported with peak efficiencies between 70% and 90% [20]–[24]. However, most of these integrated designs operate at voltage below 5 V. Here is considered the implementation of a high input voltage SC converter using a HV CMOS technology with the following targeted nominal operating point: 1 mA output load, 12 V input voltage, and 1/3 conversion ratio for 3.3 V regulation. The core of the SC converter is presented in Fig. 10(a). It is a two-phase SC converter that has been designed for 5 mA maximum output load, 5 to 12 V input voltage, and adjustable conversion ratio (1/3, 1/2 or 2/3) to provide some flexibility depending on the available inductive power and the required output voltage. The SC converter core is composed of 8 HV power transistors (M0–M8) and three capacitors C1 to 3, C3 being the output load capacitance. The SC converter is driven by two complementary nonoverlapping clocks CLK1 and CLK2. As shown in Table I, driving signals S1 to S3 are connected to CLK1, CLK2, or VPP depending on the desired conversion ratio. Initially, using the 13.56 MHz carrier as the switching frequency was considered as it would allow using on-chip capacitors. However, a satisfactory compromise between resistive and switching losses could not be reached. Large 12 V gate transitions lead to high switching losses at that frequency. Still, the HV transistor's W/L must be large enough to reduce Ron, which inevitably increases the transistor area and consequently

TABLE I
SC DC/DC CONVERTER CLOCK SETTING

Conversion Ratio	S1	S2	S3
1/3	VPP	CLK2	CLK1
2/3	CLK1	VPP	CLK2
1/2	CLK1	CLK2	VPP

its parasitic capacitances. Priority given to efficiency rather than total integration, off-chip capacitors are used instead and the switching frequency is reduced down to 50 kHz. Reducing the frequency has also the advantage of producing ripple at a low frequency that could be rejected more easily by a regulator compared to 13.56 MHz ripple that requires high value filtering capacitors. For that purpose, a low-power three stage ring oscillator (300 kHz) and a frequency divider (1:8, 1:6, 1:4 or 1:2) operating up to 12 V, have been designed to provide the SC converter with a full rail switching clock at 37.5, 50, 75 or 150 kHz. The different SC converter configurations during charging and discharging phases are given in Fig. 10(b)–(d), for the three possible step-down ratios. In the case of a 2/3 step-down ratio for example, during the charging phase, capacitors C1 and C2 are connected together in parallel, but in series with the load capacitor C3. During the discharge phase, C1 and C2 are connected together in series, but in parallel with C3. Assuming steady state, the voltages across C1 and C2 (Vc1 and Vc2 respectively), must satisfy the following equations: $\mathrm{Vc1} = \mathrm{Vc2}$, $\mathrm{Vout} + \mathrm{Vc1} = \mathrm{VPP}$, and $\mathrm{Vc1} + \mathrm{Vc2} = \mathrm{Vout}$. This leads to $\mathrm{Vout} = (2/3) * \mathrm{VPP}$. The SC converter transistor sizes have been optimized together with their gate drivers in order to maximize efficiency between 1- and 3-mA output loads, at 1/3 conversion ratio, and 12-V input, while making sure that efficiency is not degraded at other conversion ratios. This SC converter is meant to be used with a fixed conversion ratio that can be adjusted initially according to the available VPP and required VDD supplies.

IV. EXPERIMENTAL RESULTS

The proposed building blocks were fabricated in three integrated circuits (IC1 to 3) in DALSA C08E technology. Their micrographs are presented in Fig. 11 where the implemented blocks are identified. Total silicon area including input/output pads is 6, 9 and 9 mm^2 for IC1 to 3 respectively. In fact, IC3 includes other circuits than the stimulation stage, which are not used in this case but they take most silicon area as shown in Fig. 11(c). Eventually, IC3 can be redesigned to include a higher number of stimulation stages as well as a monitoring stage. In IC1 and 2, there is one ground ring but no HV supply ring. However, IC1 has a 5 V maximum VDD ring section dedicated to data recovery low-voltage I/Os. All fabricated ICs were separately tested and characterized. Here are presented measurement results for the rectifier, the voltage limiter, data recovery, and the SC converter.

Fig. 12 is an oscilloscope capture showing the unregulated bridge rectifier output (DCout) which reaches around 15 V with 22 V peak-to-peak single-ended ac inputs (Vac1 and 2). In this measurement, the output load is 1 mA only but the rectifier appears to be heavily loaded compared to simulation. Indeed,

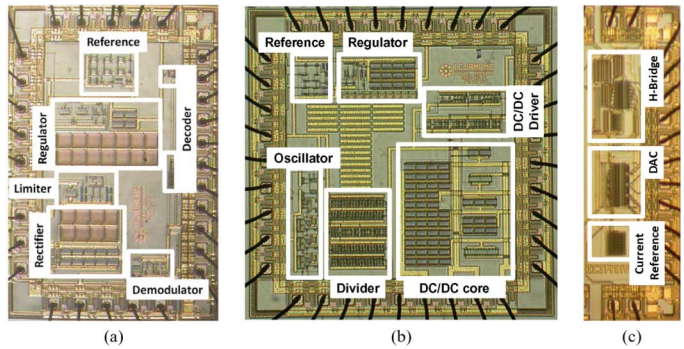

Fig. 11. Micrographs of (a) IC1, (b) IC2, and (c) IC3.

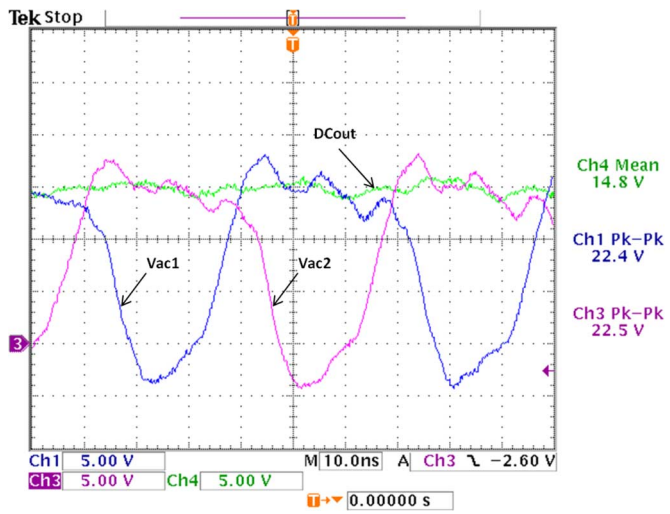

Fig. 12. Oscilloscope capture of the bridge rectifier in IC1 at 1-mA and 1-μF output load.

when Vac2 gets lower than GND while Vac1 is higher than DCout, Vac1 quickly drops down to DCout instead of charging the 1-μF output capacitance and raising DCout. In addition, Vac2 reaches a negative peak of 4 V below ground, meaning that Vac2 input pad diode is largely forward-biased, and indicating that a large current flows through the grounded substrate. The pad ESD protection diodes are clearly insufficient to keep the ac inputs higher than one threshold below ground at such high frequency, as observed in simulation. At higher output loads, latch-up also occurs as in our previous rectifier designs, but seems to be much less frequent. Latch-up may occur at the P+ diffusion of one of the cross-coupled transistors (P11 and P12 in Fig. 6) if the corresponding ac input gets higher than their bulk voltage which is connected to VH. However, when adding external lower threshold discrete diodes in parallel to the ac input pad diodes, no latch-up occurs at all. This confirms that the implemented PMOS half-bridge structure is immune to latch-up, and when the latter occurs in this design, it most probably involves the N+ diffusion in the ESD protection diodes of ac input pads. Latch-up issue still needs to be investigated further but this hybrid rectifier remains an interesting solution in our case considering targeted packaging dimensions. It performs well by providing up to 50 mW with less ripple than a fully discrete bridge rectifier. For future work, the remaining NMOS half-bridge structure should prevent the ac inputs from

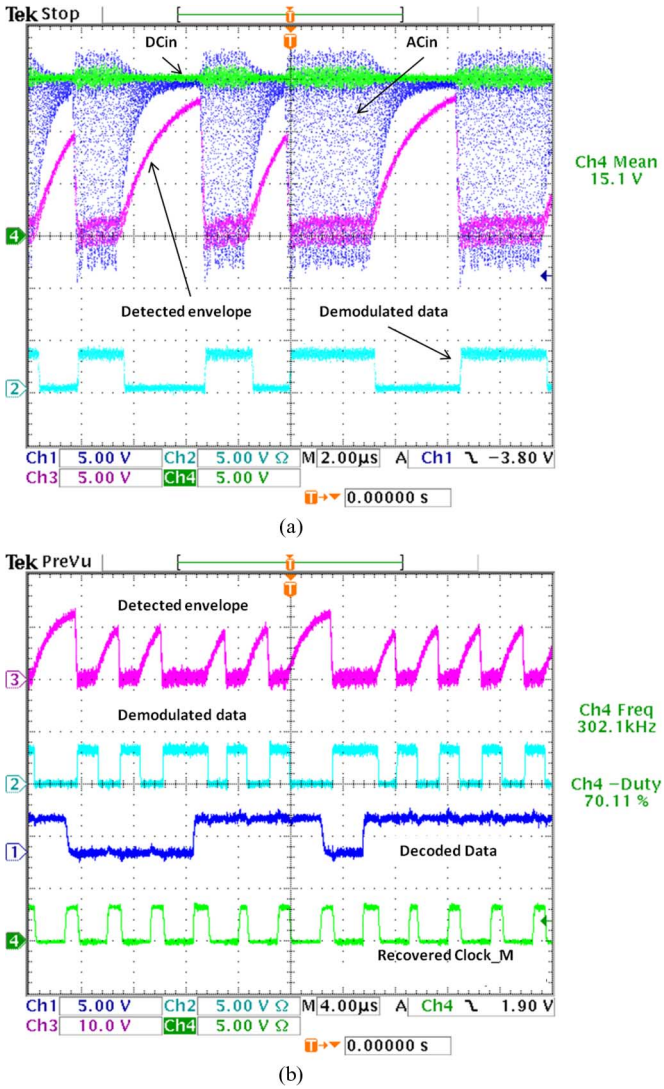

Fig. 13. Oscilloscope captures of data recovery. (a) OOK demodulation. (b) Manchester decoding.

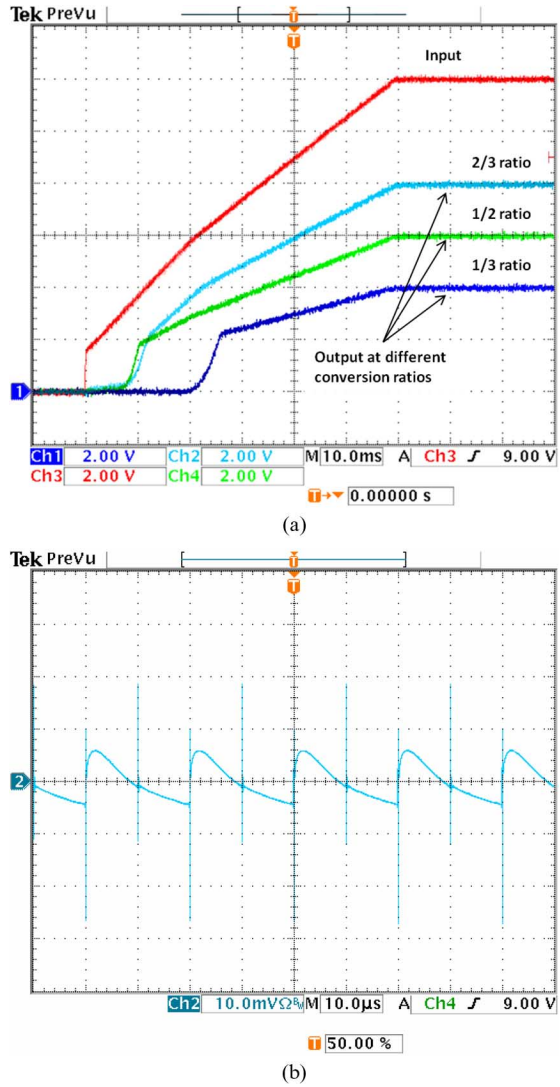

Fig. 14. Oscilloscope capture of the DC/DC converter (a) start-up with 12 V input step, and (b) worst case output ripple (∼50 mV peak-to-peak).

forward-biasing the pad diodes or else pads with no ESD protection should be used. Cross-coupling NMOS instead of PMOS transistors may also be considered to keep ESD protection.

The voltage limiter is operating as simulated with the exception of some process deviation. In order to obtain the same I-V characteristics presented in Fig. 8, the external resistor Rclamp should be set to 1340, 1220, or 1080 kΩ instead of the simulated values 1000, 900, or 800 kΩ respectively. Current consumption is less than 15 μA at 15 V, and, being slow, this voltage limiter can certainly not be used to limit directly the high-frequency inductive inputs. Thus, it is placed at the output of the rectifier making the cross-coupled PMOS transistors of the latter play an important role in limiting the output as well as the input voltages.

Data recovery is fully functional and oscilloscope captures of Fig. 13 illustrate OOK demodulation and Manchester decoding operations. If the "Detected envelope" signal follows too closely the ACin lower envelope, demodulation errors occur because of the carrier noise. Thus, the "Detected envelope" rising time must be increased (adjusted) to an optimum in order to cope with a large DCin range. This can be done by adding an external resistor in parallel with R0 in Fig. 9. The recovered "Clock_M" duty cycle must also be externally adjusted to an optimum to avoid decoding errors. In Fig. 13(b), it is around 70% but this Manchester clock remains noisy and serves only for "Demodulated data" sampling. The rest of the system will use a more stable clock provided by the ring oscillator in IC2. Note that in our previous design, the OOK demodulator was not functional while the only difference is that the diode-connected transistor M0 in Fig. 9 was implemented as a LDMOS. This also confirms that the LDMOS was not suitable in previous rectifier designs.

The SC converter output impedance ranges from 40 to 315 Ω, and is around 75 Ω at the nominal operating point. Fig. 14(a) shows the SC converter start-up with 12 V input step at different conversion ratios, while Fig. 14(b) shows the worst case output ripple observed with 2/3 conversion ratio at maximum input voltage and maximum current load (12 V, 5 mA). Fig. 15 compares measurement and post-layout simulation results of the converter power efficiency, at different input voltages, conversion ratios and load currents. Switching frequency is 50 kHz,

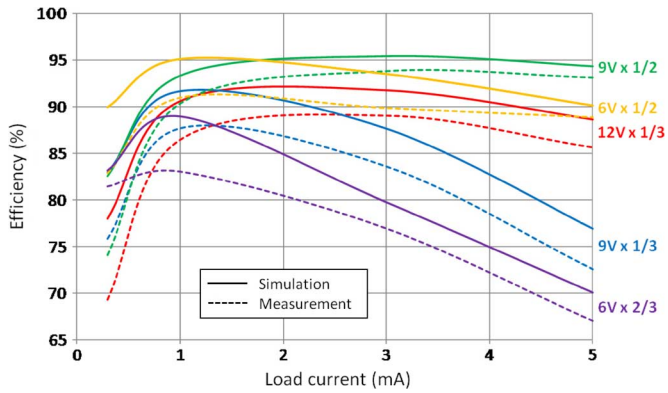

Fig. 15. The DC/DC converter power efficiency versus load current at different conversion settings. (Conditions: 1 μF output load, 50 kHz switching frequency, 200 nF flying capacitors.)

TABLE II
THE DC/DC CONVERTER OUTPUT VOLTAGE VERSUS LOAD CURRENT AT DIFFERENT CONVERSION CONDITIONS

Input voltage x Conversion ratio	Load current (mA)			
	0.3	1	3	5
12 V x 1/3	3.95	3.90	3.74	3.56
9 V x 1/3	2.96	2.88	2.63	2.00
9 V x 1/2	4.45	4.42	4.30	4.28
6 V x 1/2	2.97	2.91	2.75	2.69
6 V x 2/3	3.81	3.55	3.16	2.74

load capacitance is 1 μF, and flying capacitors (C1, C2) are 200 nF. Post-layout simulations were carried out taking into account parasitic capacitances and bonding pads. Table II presents the converter output voltage with respect to the load current at different conversion settings. The SC converter power efficiency reaches a maximum of 94% and is around 86% at the targeted nominal operating point (1 mA load, 12 V input, and 1/3 conversion ratio). With such efficiency, the proposed step-down inductive power recovery topology is more advantageous than its step-up counterpart. The SC converter power efficiency calculation takes into account the power consumption of the ring oscillator, frequency divider, nonoverlap clock generator and driver. The efficiency drops at higher loads because of resistive losses, in particular with a 6 V input voltage. Indeed, some mid-rail power transistors are not sufficiently switched-on. This is the case of PMOS transistor M4 for example at 2/3 conversion ratio setting during the discharge phase. Its gate is attached to GND while its source is connected to a voltage node lower than 2 V ($\mathrm{Vc1} = \mathrm{Vout}/2 = \mathrm{VPP}/3$). The threshold voltage being around 1 V, the M4 transistor Vgs is clearly not high enough. For the same reasons, the output voltage also drops for higher loads.

At the system level, measurements demonstrated that with 50 mW available inductive power, the power recovery front-end has an overall power efficiency of around 78.8% when delivering 3 mA, 1 mA and 100 μA from 12 V, 3.3 V and 1.2 V supplies respectively. In that situation, the inductive voltage is around 12.66 V and still has enough room for 12 V regulation. When no current is drawn from the 12 V supply, the inductive voltage rises up to 20 V and the voltage limiter shunts around 1.55 mA. In that case, the 6.8 uF filtering capacitor is charged

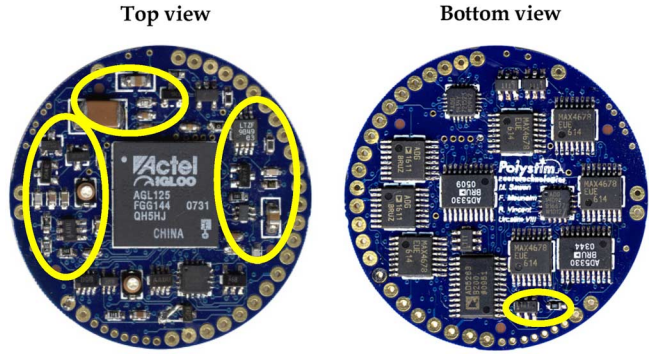

Fig. 16. Discrete components based neurostimulator's PCB (∅38 mm) with power and data recovery front-end area encircled.

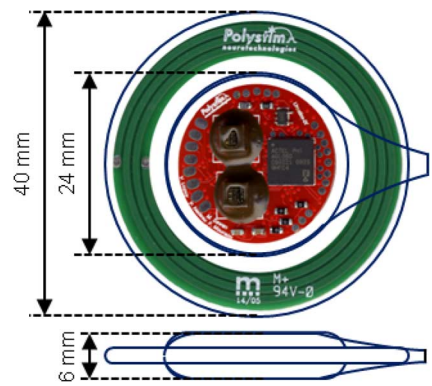

Fig. 17. Highly-integrated neurostimulator's PCB (∅21 mm) and proposed packaging dimensions in case of a larger coil (∅38 mm).

with 50 μC which can provide 3 mA stimulation for more than 16 ms for example. Depending on stimulation parameters, this can translates to lower required inductive power or smaller required antenna diameter.

For comparison, the discrete components based neurostimulator prototype shown in Fig. 16 is 38-mm diameter and hosts a FPGA with 12 $\times$ 12 Fine Pitch Ball Grid Array (FBGA) of 13 $\times$ 13 mm dimensions and 1 mm pitch. The inductive power and data recovery front-end occupies a large PCB area as encircled in Top and Bottom views of Fig. 16. Because of the large number of discrete components, this PCB required eight layers and numerous blind vias for a complete routing of the system. The highly-integrated neurostimulator's PCB has been designed but not fabricated at this stage because the rectifier in IC1 still suffer from latch-up and IC3 will be redesigned to include multiple stimulation stages. However, the nonfunctional mock-up PCB shown in Fig. 17 has been fabricated to evaluate assembly challenges and final packaging dimensions. This PCB is 21-mm diameter and can host a small FPGA in a 11 $\times$ 11 Chip Scale Package (CSP) of 6 $\times$ 6 mm dimensions and 0.5 mm pitch. It has much less components count but the limited space and the 0.5 mm pitch FPGA makes it more difficult. Bare dies of IC1 and IC2 are mounted with the die-on-PCB assembly approach and connected with direct bonding to pads. Four bare dies of IC3 can be assembled in two pairs with the die-stack approach. For chronic animal implantation, the prototype will be packaged in two layers of different materials. The first layer is a rigid epoxy that protects the implant from infiltration of fluids

and offers a reliable isolation for the electronic components. The second layer is a biocompatible silicone that offers a soft contact for corporal tissues. Fig. 17 shows the targeted packaging form and dimensions. This neurostimulator can be packaged in even smaller form factor with a smaller diameter coil in case of lower inductive power requirements, and can be considered in numerous other neurostimulation applications such as epilepsy treatment, pain release, etc.

V. Conclusion

This paper presented a highly-integrated neurostimulator prototype based on three custom ICs fabricated in HV CMOS technology, a commercially available FPGA, and a few count of discrete components. The inductive power and data recovery front-end was fully integrated in two ICs, adopting an unconventional step-down approach where the inductive voltage is left free up to 20 V. The architecture and the design of key building blocks such as the bridge rectifier, the voltage limiter, the DC/DC converter and data recovery were presented. Measurement results confirm good overall functionality even if the integrated HV rectifier requires further investigation of latch-up occurrence at higher loads. More importantly for the proposed topology, the DC/DC converter power efficiency is around 86% at the targeted nominal conditions making the step-down power recovery approach more advantageous than its conventional step-up counterpart.

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