Integrated High-Voltage Inductive Power and Data-Recovery Front End Dedicated to Implantable Devices

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***Abstract*—In near-field electromagnetic links, the inductive voltage is usually much larger than the compliance of low-voltage integrated-circuit (IC) technologies used for the implementation of implantable devices. Thus most integrated power-recovery approaches limit the induced signal to low voltages with inefficient shunt regulation or voltage clipping. In this paper, we propose using high-voltage (HV) complementary metal–oxide semiconductor technology to fully integrate the inductive power and data-recovery front end while adopting a step-down approach where the inductive voltage is left free up to 20 or 50 V. The advantage is that excessive inductive power will translate to an additional charge that can be stored in a capacitor, instead of shunting to ground excessive current with voltage limiters. We report the design of two consecutive HV custom ICs—IC1 and IC2—fabricated in DALSA semiconductor C08G and C08E technologies, respectively, with a total silicon area (including pads) of 4 and 9 mm^2, respectively. Both ICs include HV rectification and regulation; however, IC2 includes two enhanced rectifier designs, a voltage-doubler, and a bridge rectifier, as well as data recovery. Postlayout simulations show that both IC2 rectifiers achieve more than 90% power efficiency at a 1-mA load and provide enough room for 12-V regulation at a 3-mA load and a maximum-available inductive power of 50 mW only. Successful measurement results show that HV regulators provide a stable 3.3- to 12-V supply from an unregulated input up to 50 or 20 V for IC1 and IC2, respectively, with performance that matches simulation results.**

***Index Terms*—Bridge circuits, complementary metal–oxide semiconductor (CMOS) integrated circuits, high-voltage techniques, implantable biomedical devices, inductive power transmission, rectifiers, regulators.**

I. Introduction

CHRONIC implantation of biomedical power-consuming devices requires wireless power transmission through inductive links in order to avoid the limited operation lifetime of batteries. In some applications, such as neurostimulation for bladder rehabilitation, a near-field inductive link may be the only possible solution to provide sufficient power to address the large electrode-nerve impedance and high-current stimulation requirements. However, during low-current consumption periods, the inductively recovered voltage may largely exceed the low-voltage integrated circuits (ICs) compliance. To protect the system from these high voltages, power-recovery circuits use voltage limiters either on-chip using voltage clipping, or off-chip using discrete components, such as Zener diodes or shunt regulators [1], [2]. These approaches are usually not energy efficient and this was the case of the most recently published system architectures [3]–[5], where a shunt regulator was used to limit the rectified voltage to 3.3 or 5 V as shown in Fig. 1. Using inductively coupled spiral antennas, energy is transmitted to the implant by an external controller. The transmitted energy is recovered as the parallel LC network resonates at a carrier frequency of 13.56 MHz. This frequency is chosen within the industrial-scientific-medical (ISM) radio band so that coupling attenuation through the skin tissues remains acceptable with the use of 4-cm diameter antennas. The inductive voltage is then rectified and filtered with the capacitor $\mathrm{C_{filter}}$ which also can be seen as the energy storage for the implant. The shunt regulator was mainly chosen to provide a simple voltage limiting option with small space requirements in a discrete implementation. However, the regulator must be adjusted according to the worst case so that it remains capable of providing the maximum required stimulation current when available inductive energy is minimal. Since the inductive voltage is limited, any excessive inductive power that is not used by the system will be heat-dissipated by the shunt regulator because the resulting excessive current will be simply shunted to ground.

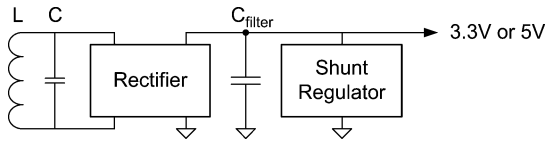

Fig. 1. Inductive power recovery with simple shunt regulation.

Moreover, the 5-V supply turned out to be insufficient over time in recent chronic dog experiments as the cuff-electrode/nerve interface impedance may become higher than 4 kΩ eight months after implantation. Consequently, the stimuli generator supply must be increased to at least 9 or 10 V to provide the 2-mA required stimulation current to these high electrode impedances. The rest of the system should still run at 3.3 V or lower to reduce power consumption.

Assuming that the rectified voltage is limited by a shunt regulator, there are two possible approaches in order to provide dual

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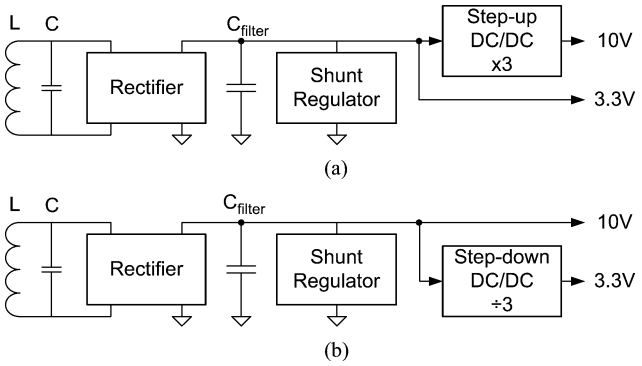

Fig. 2. Inductive power-recovery topologies. (a) Step up. (b) Step down.

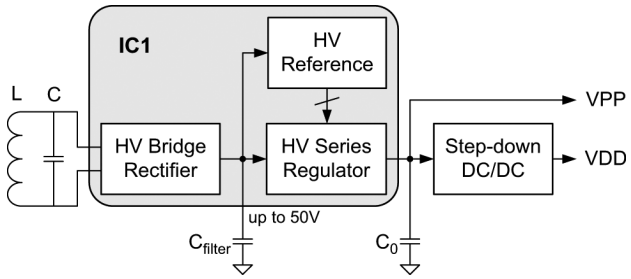

Fig. 3. Proposed power-recovery topology with integrated IC1.

supplies (Fig. 2). These approaches are based on voltage step-up and step-down topologies, where switched-capacitor dc/dc converters are used to provide better efficiency. The step-up approach is preferred in general and is used in most inductively powered systems since minimizing the inductive voltage would improve efficiency. However, when considering the total efficiency of the system, it is not a trivial task to select the most advantageous topology [6]. If the shunt regulator and the rectifier efficiencies are disregarded, the following parameters should be taken into account: the load current on each supply, the inductive-link secondary equivalent source resistance (Rs), as well as the converters' efficiencies in those conditions. Considering the actual conditions of a bladder neurostimulator (more than 1-mA system current consumption from 3.3 V, up to 2-mA stimulation pulses from 10 V and $\mathrm{Rs} = 12.36\ \mathrm{k}\Omega$) and applying the theoretical study published in [6], the step-down approach would be more efficient if the converter efficiency is higher than 40% and its output impedance is less than 12 kΩ. The latter is normally satisfied since the output impedance of dc/dc converters is generally of the order of 100 Ω. Thus, the step-down approach is worth being investigated in this case with a dc/dc converter of at least 40% efficiency.

In addition to the step-down approach, it is possible not to limit the rectified voltage at all by using high-voltage (HV) technology. The advantage would be that excessive inductive power will translate to an additional charge that can be stored in the filtering capacitor, leading to a higher rectified voltage. This additional charge can be used to provide higher stimulation pulse current for a given pulse duration if needed and that without additional inductive power. With voltage limiting, excessive inductive power is simply heat dissipated as it translates to an excessive current that is shunted to ground. Thus, the shunt regulator of Fig. 2(b) can be replaced by an HV buck converter that can cope with a variable input and still offer the best efficiency and regulation. Yet, unless the feasibility of a high-frequency HV buck converter using an integrated inductance is demonstrated without degraded performance, it remains unsuitable since it requires a high value discrete inductor that does not favor integration and miniaturization. As an alternative and a better compromise between the shunt regulator and the buck converter, an HV series regulator can be used as shown in Fig. 3. The rectified voltage will not be limited by the series regulator as in the case of the shunt regulator, but will rather be limited indirectly by the maximum-available inductive power and the minimum system power consumption, including power dissipated by the series regulator.

This paper proposes the implementation of the inductive power and data-recovery front end in HV CMOS technology using a step-down approach where the rectified voltage is left free as shown in Fig. 3. The fabrication cost with HV CMOS technology may be relatively higher than standard processes, but it is becoming widely used in many applications, such as flat-panel displays, micro-mirrors, microfluidics, and microelectromechanical systems (MEMS) in general. The design of two consecutive HV custom ICs (IC1 and IC2) is reported. They have been fabricated in DALSA Semiconductor C08G and C08E technologies, respectively. Both ICs include HV rectification and regulation; however, IC2 includes two enhanced rectifier designs—a voltage-doubler and a bridge rectifier—as well as a data-recovery block. In fact, preliminary results were presented in [7] and [8], which are elaborated in this proposed work. The remainder of this paper presents the design of the fabricated ICs and compares postlayout simulation with measurement results.

II. Designs Description

As a first step toward full integration of the power-recovery stage, a first IC (IC1) has been designed and implemented in C08G technology, which is able to operate at drain-source voltages (Vds) as high as 300 V. As shown in Fig. 3, IC1 includes three main HV building blocks: 1) bridge rectifier, 2) series regulator, and 3) voltage reference—all can be driven by an input voltage as high as 50 V. Due to the gate-source voltage (Vgs) limitation to 5 V of the C08G technology, no special design technique could be used for the bridge rectifier in IC1 to improve its efficiency and protect its transistors from latch-up or substrate leakage current. The Vgs limitation also proved to be a major obstacle for the design of an efficient dc/dc converter. For those reasons, we changed our target technology to C08E which can operate at Vgs up to 20 V even if Vds is also limited to 20 V. The block diagram of Fig. 4 shows the second IC (IC2) within the proposed inductive power and data-recovery front end.

IC2 includes similar building blocks as IC1 but offers two enhanced rectifier designs—a voltage-doubler and a bridge rectifier—as well as a data-recovery circuit. Depending on the available inductive power and the system power consumption, the inductive voltage can be rectified using either a voltage-doubler or a bridge rectifier. Both rectifier designs were implemented for comparison purposes. The rectified voltage may exceed the

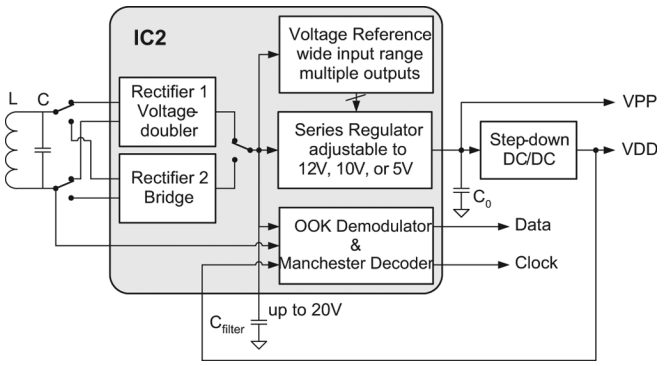

Fig. 4. Proposed power and data-recovery topology with integrated IC2.

C08E technology 20-V limit in case of high inductive coupling and a light load. Consequently, on-chip voltage clipping (not included in IC2) can be added wherever needed in a dedicated design. For an implanted neurostimulator, the presence of an HV node is safe as long as safety measures are implemented at the system level to prevent unwanted operation in case of any device failure. Thus, a maximum of 20 V is applied to the voltage reference, the series regulator, and the demodulator. The voltage reference provides stable multiple outputs over a wide input range while the series regulator provides a supply voltage (VPP) that can be adjusted to 5, 10, or 12 V. The capacitor C0 is meant for the regulator stability and additional carrier filtering. The on-off keying (OOK) demodulator and the Manchester decoder are responsible for data and clock recovery.

A. HV Bridge Rectifier in IC1

In a CMOS implementation, diodes can be replaced by diode-connected MOS transistors; however, their threshold voltage (Vth) and the voltage drop across them limit the rectifier efficiency. In order to improve efficiency, several techniques have been proposed in the literature. Cross-coupling allows decreasing the transistor ON resistance [9]–[15]. An active diode using a comparator or "smart" rectification virtually cancels the transistor Vth [9], [11]–[19]. Other techniques aim at protecting against latch-up and substrate leakage currents [10]. Using C08G technology, the implementation of these techniques has been considered for the rectifier design even if the targeted input voltage exceeds all examples in the literature. Unfortunately, the Vgs is limited to 5 V, making it a major obstacle. Designing an active rectifier in this technology requires level shifters that will affect total efficiency. In addition, these level shifters [20] are designed, in general, for a specific fixed input voltage, which is not our case. Thus, in IC1, the HV rectifier is implemented with simple diode-mounted transistors. The maximum input voltage and current are 100 V and 16 mA, respectively. The transistors are diode-connected by short-cutting the gate with the source instead of the drain because of the same Vgs limitation [21]. Among all HV transistors available in the design kit, the chosen NMOS transistor has a floating source that can go up to 100 V and gives the best overall efficiency. Using PMOS transistors led to a less efficient rectifier due to larger charge injection into the substrate.

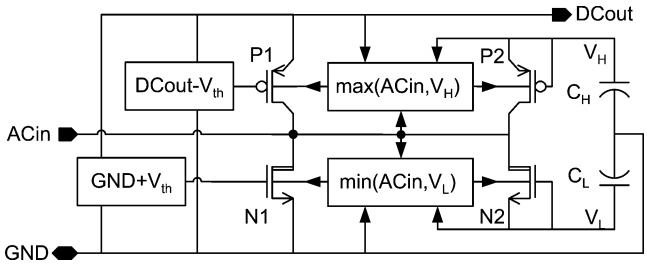

Fig. 5. Schematic of the bridge rectifier in IC2.

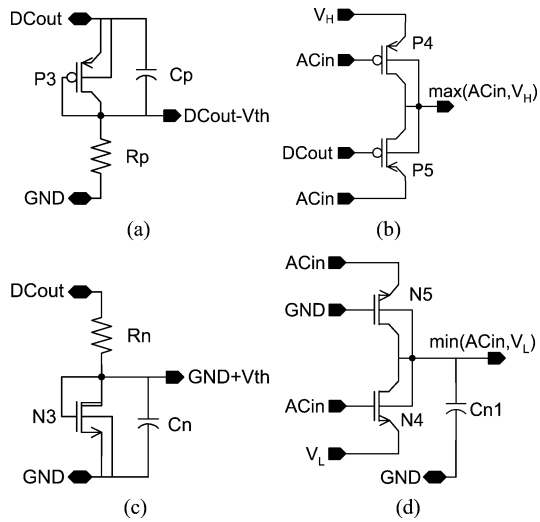

Fig. 6. Functional blocks used in Figs. 5. 7 (a) "$\mathrm{DCout} - \mathrm{V_{th}}$," (b) "$\max(\mathrm{ACin}, \mathrm{V_H})$," (c) "$\mathrm{GND} + \mathrm{V_{th}}$," and (d) "$\min(\mathrm{ACin}, \mathrm{V_L})$."

B. Voltage-Doubler Rectifier in IC2

The voltage-doubler rectifier has been a topology of choice for all of our discrete neurostimulator prototypes so far. It enables the output to reach the required dc voltage while keeping the inductive voltage low. In addition, the voltage-doubler requires only two diodes and introduces only one diode voltage drop. Therefore, with equivalent diodes, the voltage-doubler would be a more efficient solution compared to the bridge rectifier (two diode voltage drops). The schematic of the designed voltage-doubler rectifier and its building elements are shown in Figs. 5 and 6, respectively. For all figures, the HV transistor symbols of the C08E design kit are adopted. All transistors operate at Vgs and Vds voltages up to 20 V. In these figures, PMOS devices (P1-P5) and NMOS devices (N4-N5) are bidirectional with double extended channels, have threshold voltages around 1 V, and breakdown voltages above 30 V. Both devices can have a floating source (up to 20 V relative to Bulk), but NMOS devices can be isolated from the P-substrate with a deep N-well if required. While the PMOS device model is fully scalable, the NMOS model is provided either for a fixed gate length or a fixed width. NMOS devices (N1-N3) are multiples of an elementary LDMOS transistor whose layout and corresponding model are provided in the design kit with fixed dimensions. This LDMOS transistor has a low-voltage floating source (5 V max relative to bulk), a breakdown voltage of 50 V, a higher threshold voltage but a lower Ron. The core of the rectifier is formed by MOS diodes N1 and P1. Instead

of the simple diode-connected configuration [1], a technique that virtually cancels the transistor threshold is used. It results in higher rectified voltage (DCout) and higher efficiency. Capacitor Cp (Cn) holds the Vth voltage of diode P1 (N1) by replicating its threshold voltage with a matched diode P3 (N3) to track process and temperature variations [18].

Resistances Rn and Rp are made large to reduce the bias current. In order to avoid latch-up and substrate leakage current, P1 bulk was first connected to the highest of ACin and DCout, and N1 bulk to the lowest of ACin and GND [10]. However, at high load current, the voltage difference between the ACin positive peak and DCin (and similarly, the ACin negative peak and GND) becomes higher, making it difficult to follow for the bulk nodes, especially at the 13.56-MHz carrier frequency. Thus, a dummy unloaded voltage-doubler rectifier (diode connected P2 and N2) and filtering capacitors C_H and C_L are used to provide the highest and lowest possible voltages (V_H and V_L) from ACin. So transistors P4 and P5 connect the P1 bulk to V_H most of the time and to ACin when it gets higher than DCout. Similarly, transistors N4 and N5 connect N1 bulk to V_L most of the time and to ACin when it gets lower than GND. The additional capacitor Cn1 helps in filtering fluctuations transmitted through parasitic capacitances from ACin to N1 bulk. The rectifier was optimized for maximum power efficiency at 1-mA load current and input power so that output voltage is maximum without exceeding the 20-V limit. Tuning was limited by fixed NMOS transistors gate length and fixed LDMOS dimensions. The main compromise in sizing N1 and P1 is between losses due to their ON resistances (Ron) or their parasitic capacitances.

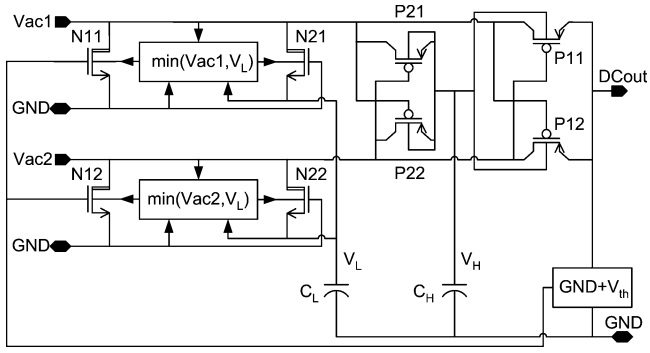

Fig. 7. Schematic of the bridge rectifier in IC2.

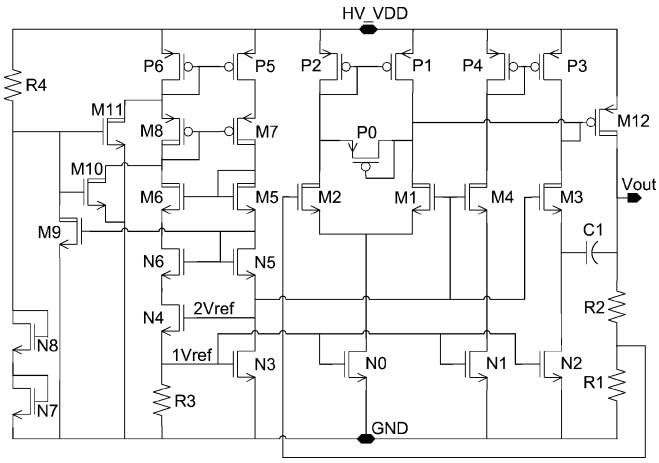

Fig. 8. Schematic of the HV series regulator in IC1 with reference and startup circuit.

C. Bridge Rectifier in IC2

Among the disadvantages of the voltage-doubler rectifier is the silicon area because of the required large transistors to reduce Ron and improve efficiency. The bridge topology benefits from opposite-phase signals that can be used to switch-on harder much smaller transistors, yet achieving the same Ron as large transistors. In addition, compared to the voltage-doubler, the full-wave bridge rectifier offers a lower output ripple and a higher equivalent input resistance. The schematic of the designed bridge rectifier is shown in Fig. 7. Its building elements are the same presented earlier in Fig. 6. The rectifier core is formed by MOS diodes N11, N12, P11, and P12. Cross-coupling the PMOS transistors (P11 and P12) allows reducing their size [9], [22]. For MOS diodes N11 and N12, the same Vth cancellation technique described earlier is used except that it is common for both transistors. Sharing the Vth cancellation circuit offers a more stable gate voltage because fluctuations of Vac1 and Vac2, which are transmitted through drain-gate parasitic capacitances, cancel each other.

A dummy unloaded bridge rectifier formed by cross-coupled transistors (P21, P22), diode-connected transistors (N21, N22), and filtering capacitors C_H and C_L provide the highest (V_H) and lowest (V_L) possible voltages from Vac1 and Vac2. Note that N21 and N22 have their gate connected to GND instead of V_L. This was advantageous in this bridge differential configuration only since it provided some Vth cancellation for N21 and N22, as opposed to simple diode-connected N2 in the voltage-doubler (Fig. 5). Using the V_L voltage, transistors N11 and N12 are protected from latch-up and substrate leakage current the same way as in the voltage-doubler. However, here, transistors (P11, P12) and (P21, P22) are protected from latch-up by connecting their bulk to V_H. This was enough to keep their bulk at the highest voltage even in high load conditions.

D. High-Voltage Series Regulators

The designed HV regulator in IC1 provides a 10-V output voltage and can deliver a maximum current of 10 mA with a maximum input voltage of 50 V. It consists of a pass transistor, a differential amplifier, a voltage reference, and a startup circuit. For low dropout, an HV-PMOS pass transistor is chosen [23]. A large output capacitor is then needed for stability to reduce the output impedance at high frequency. The total current consumption has been limited to less than 150 μA. The amplifier and the voltage reference use 5-V PMOS active loads whose N-well can support voltages as high as 300 V. The regulator schematic, with voltage reference and start-up circuit, is presented in Fig. 8. The single-stage amplifier uses HV-NMOS transistors with a floating source for the differential pair (M1-M2). The HV-PMOS pass transistor M12 is protected by limiting its Vgs to less than 5 V using the diode-connected transistor P0. This HV amplifier has been introduced by Ballan with a technique improving PSRR and compensation [24]. The PSRR

improvement is achieved by biasing transistor M3 in the saturation region with current sources (N1-N2) and the current mirror (P3-P4). In the feedback path (from output Vout to the M12 transistor gate), the impedance is very low, in the order of 1/gm of transistor M3, whereas in the feedforward path, impedance is very high, in the order of 1/gds of transistor M3.

Thus, the direct path of power-supply variations is interrupted while feedback and compensation remain functional. The C08G kit does not offer the possibility of changing the HV transistors dimensions. Consequently, the design optimization of this amplifier is difficult since it is not possible to adjust the transistors parameters. This is especially the case since performance and stability, in particular, must be ensured over a large input voltage range. It has also been ensured that the critical node, which is the M12 gate, does not go below 5 V relative to the input voltage. This has been verified in different situations of process corners, temperature, and power supply as well as in static and dynamic conditions. The most critical dynamic situation corresponds to power-on with a steep input voltage step from 0 to 50 V. The gate of transistor M12 is then protected as long as the power supply rising time is higher than a certain value. If needed, the rising time of the rectified voltage can be increased with a larger filtering capacitor.

The voltage reference circuit uses a Vgs-referenced supply-independent technique as described in [25] and [26]. The Vgs of transistor N3 is applied across a 100-kΩ resistor (R3). When the power supply increases, P5 Vds increases and so does the current in that branch. Consequently, N3 Vgs and the resistor current increase as well. With optimization, N4 Vgs can decrease and compensate for the increase of N3 Vgs. If temperature dependency is neglected, this autocompensation mechanism allows the circuit to provide very stable voltage references (1Vref, 2Vref) with respect to supply variations over a large voltage range [25]. However, to support higher voltages, HV cascode transistors are used [24]. In Fig. 8, those are NMOS (M5, M6) and PMOS (M7, M8) transistors. The resulting high-voltage reference consumes 20-μA total current, operates up to 50 V, and makes the design of the presented HV regulator possible. In addition, a startup circuit is mandatory in order to place the reference at the desired operating point at power-on. During startup, the gates of transistors M10 and M11 are pulled up toward the supply by R4, but are limited by protection diode-connected transistors N7 and N8. Thus, transistors M10 and M11 activate the reference since they are initially closed and pull down the gates of transistors P5, P6, M7, and M8 to ground. As soon as the gate of M9 reaches the threshold voltage, the gates of M10 and M11 are pulled down to ground and the startup circuit is deactivated. R4 is a large resistor ($\sim 5\ \mathrm{M}\Omega$) that is made of highly resistive Polycap P-type material with a serpentine layout. With a maximum supply of 50 V, the startup branch will consume 10 μA at most. An external resistor can be added in series to increase the resistance value and reduce even more current consumption if needed.

The voltage reference and series regulator design in IC2 is similar to that in IC1 except that no gate protection is necessary in this case. In addition, all transistors used in the IC2 regulator are bidirectional with double extended channels that can operate at Vgs and Vds up to 20 V with a breakdown voltage above 30 V.

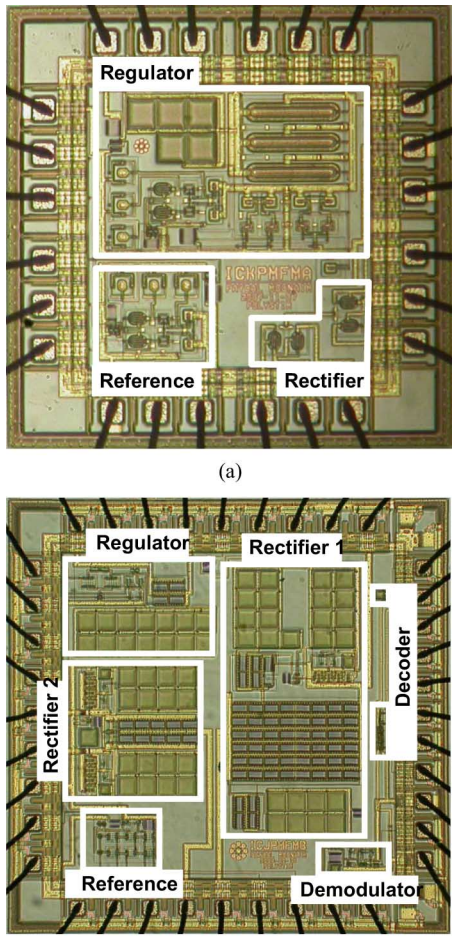

Fig. 9. Micrographs of (a) IC1 and (b) IC2.

The IC2 regulator design optimization was easier than in IC1 because the PMOS device model in the C08E kit is fully scalable and the NMOS model is provided either for a fixed length or a fixed width.

III. Simulation and Measurement Results

The designed and implemented chips IC1 and IC2 have been fabricated in DALSA C08G and C08E technologies, respectively. Their micrographs are presented in Fig. 9 where the implemented blocks are identified. Total silicon area including input/output (I/O) pads is 4 mm^2 and 9 mm^2 for IC1 and IC2, respectively. In both ICs, there is one ground ring but no high-voltage supply ring. However, IC2 has a 5-V maximum VDD ring section dedicated to data-recovery low-voltage input/outputs (I/Os). In IC1, the upper part of the chip corresponds to the HV regulator that includes a voltage reference and a startup circuit. The pass transistor M12 is in the upper-right and is made of three parallel HV-PMOS, while the compensation capacitor C1 is in the upper left (Fig. 8). The diode-connected bridge rectifier and a duplicated voltage reference for testability are in the lower part of the chip. In IC2, the HV regulator in the upper left does not include the voltage reference but gives access to N0 and M1 gates (Fig. 8) to set the amplifier tail current and input reference.

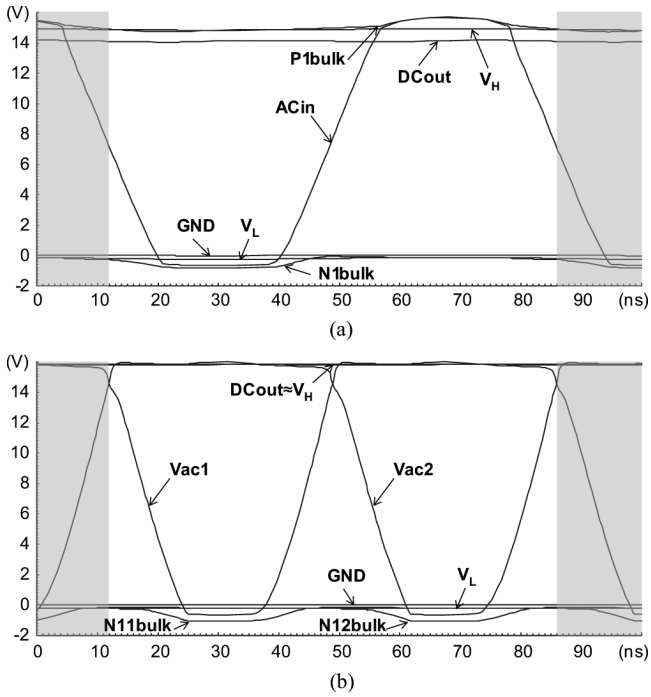

Fig. 10. Postlayout simulation of (a) the voltage-doubler and (b) bridge rectifiers in IC2.

The voltage reference has been implemented as stand-alone block to be shared by other circuits in the system, such as the dc/dc converter in particular. The bridge rectifier (Rectifier 2) silicon area is around half that of the voltage-doubler (Rectifier 1). Both rectifiers' areas comply with the space requirements of the targeted neurostimulator prototype which will be assembled on a 21-mm printed-circuit board (PCB) diameter.

A. Rectifiers

Table I presents the expected IC1 rectifier power efficiency from postlayout simulations that include extracted parasitics. In all presented simulations and measurements results, power efficiency is calculated by using the following equation:

$$\eta = \frac{V_{\text{out}} \cdot I_{\text{out}}}{P_{\text{in}}}$$

where V_{out} is the dc output voltage or its average value in the presence of large ripple, I_{out} is the dc load current and P_{in} is the average value of the instantaneous product of input voltage and input current. Measurements showed that the rectifier is prone to high substrate leakage current and latch-up. Even though the rectifier may appear functional at first, high ripple on the rectified output and high input current indicate the presence of substrate leakage currents. After a random time, latch-up occurs and the rectifier heavily loads the input source especially when using a limited power inductive link. Fig. 10 presents postlayout transient simulations of the IC2 voltage-doubler and bridge rectifiers, at 13.56 MHz, 3-mA output load, and 50-mW input power. The time window of around 74 ns represents one single period of an unmodulated carrier signal that is single ended (ACin) or differential (Vac1, Vac2) for the voltage-doubler and bridge rectifiers, respectively. Fig. 10(a) shows how P1 (N1) bulk remains higher (lower) than ACin when ACin becomes higher (lower) than DCout (GND). Similarly, in Fig. 10(b), N11 (N12) bulk remains lower than Vac1 (Vac2) when Vac1(Vac2) gets lower than GND.

TABLE I
POSTLAYOUT SIMULATION OF THE IC1 RECTIFIER POWER EFFICIENCY AT DIFFERENT INPUT AND LOADING CONDITIONS

Power efficiency (%)		Output load (Ohms)				
		500	5K	50K	500K	5M
Input voltage	50 V	49	82	91	80	29
	30 V	48	80	89	77	26
	10 V	40	68	77	68	21

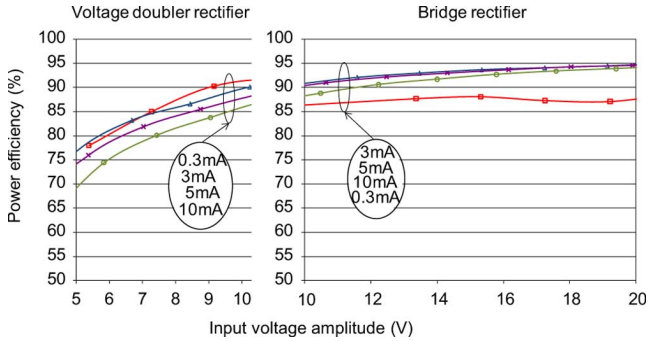

Fig. 11. IC2 Rectifiers power efficiency postlayout simulation results.

TABLE II
IC2 RECTIFIERS COMPARISON AT 13.56 MHZ AND THREE LOADING CONDITIONS: 0.3, 1, AND 3 mA, POSTLAYOUT SIMULATION RESULTS

Rectifier	Voltage-doubler			Bridge rectifier		
Output load (mA)	0.3	1	3	0.3	1	3
Input power (mW)	6.6	22.1	50	7	21	50
Input voltage amplitude (V)	10.7	11.1	8.2	20	20	16.8
Output voltage (V)	20	20	14.3	19.6	19.4	15.5
Output ripple (mV peak-to-peak) (C_{filter} = 1nF)	50	84	125	15	29	74
Power efficiency (%)	90.6	90.5	85.7	83.8	92.3	93.1

Rectifiers are often compared with respect to the voltage conversion ratio. However, due to the voltage-doubler, power efficiency is more appropriate for comparison. Table II and Fig. 11 compare power efficiency simulation results for the voltage-doubler and bridge rectifiers in different loading conditions. The target load range is 0.3 to 1 mA, to which a stimulation pulse current adds a maximum of 2 mA. Both rectifiers have been optimized for this range but may provide a maximum current of 10 mA with higher input power. In Table II, the sinusoidal input amplitude was adjusted to achieve the highest rectifier output voltage without exceeding 20 V at the rectifier input or output. We assume that voltage limiting will be provided to protect the chip either with voltage clipping or shunt regulation. In addition, our target inductive coupling conditions lead to a maximum-available inductive power of 50 mW. So these simulations take into account those two limits, and shaded cells in Table II indicate when they are reached.

In terms of power efficiency, both rectifiers are equivalent at a 1-mA load, but the bridge is more efficient at higher loads while the voltage-doubler is more efficient at lower loads. In terms of output voltage, the bridge rectifier provides a higher voltage at high loads, but both provide enough room for 12-V regulation at a

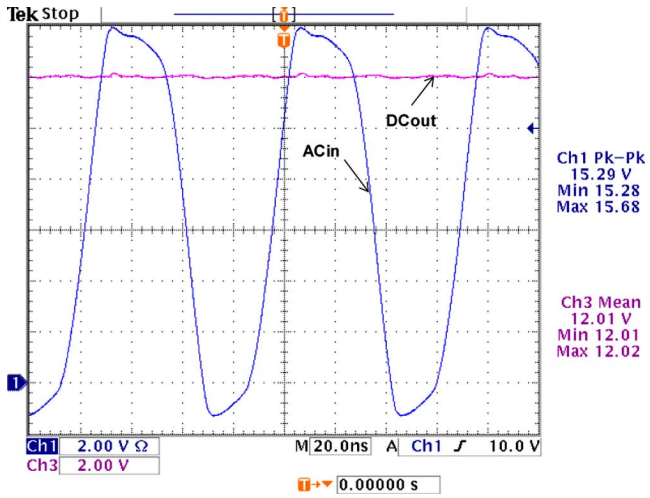

Fig. 12. Oscilloscope capture of the voltage-doubler rectifier at 13.56 MHz and 15 V peak-to-peak single-ended input and 1-mA and 1-μF output load.

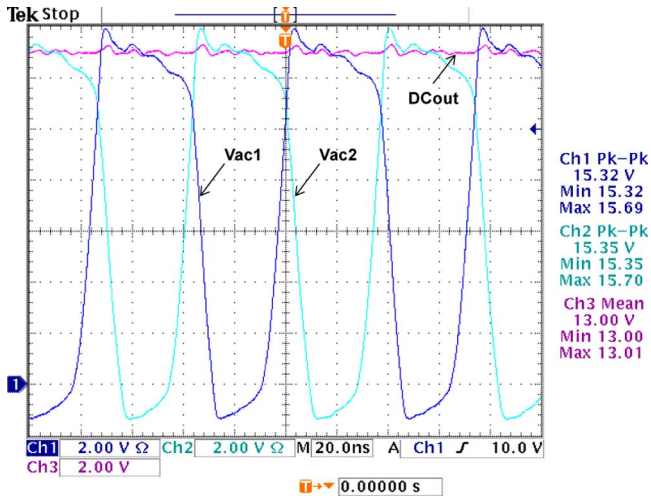

Fig. 13. Oscilloscope capture of the bridge rectifier at 13.56-MHz and 15-V peak differential input and 1 mA and 1-μF output load.

3-mA load. The voltage-doubler may look advantageous since it requires a lower input voltage but this also means that the required input current is doubled. In fact, the equivalent input impedance of the bridge rectifier is around 3 to 4 times higher than that of the voltage-doubler. Thus, for maximum power transfer, the inductive antenna should be characterized in order to evaluate the LC equivalent series resistance at the carrier resonance frequency, and the rectifier topology should be chosen according to best impedance matching. Figs. 12 and 13 are oscilloscope captures showing the inputs and outputs of the voltage-doubler and bridge rectifiers, respectively, at 13.56 MHz and the 1-mA output load. Important differences with simulations can be noticed. First, when the voltage-doubler ac input becomes higher than DCout or lower than GND, it reaches a peak that is higher than the dropout voltage seen in simulations. The bridge differential inputs also show that peak, but more important, they are abnormally loaded when they become higher than DCout, while the output load is only 1 mA. This is a clear indication of substrate leakage current. Moreover, when investigating different input and loading conditions, latch-up also occurs at higher loads and higher voltages. Fig. 14 compares simulation and measurement results for

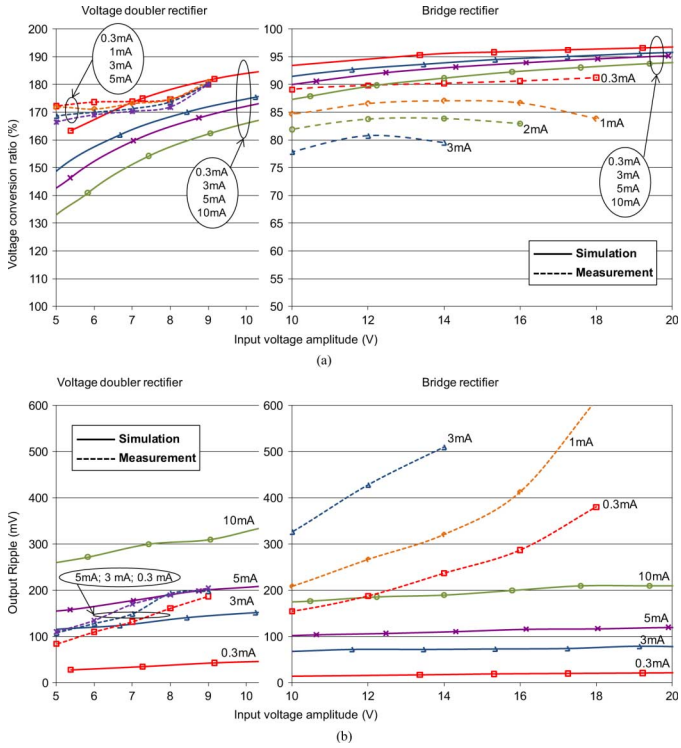

Fig. 14. IC2 rectifiers' (a) voltage conversion ratio and (b) output ripple as well as postlayout simulation and measurement results.

the voltage conversion ratio and output ripple for both rectifier designs. The voltage conversion ratio is calculated as $V_{\rm out}/V_{\rm in}$, where $V_{\rm out}$ is the dc output voltage or its average value in the presence of large ripple and $V_{\rm in}$ is the ac input voltage (peak) amplitude, considering a single-end input for the voltage-doubler and a differential input for the bridge rectifier. Measurements are provided only in conditions where latch-up did not occur. At low load, the bridge rectifier conversion ratio is close to simulation but drops as the load is increased. The bridge rectifier ripple is also much higher than simulation and increases with input voltage and load current. Both deviations from simulation can be explained by the substrate leakage current. However, the voltage-doubler conversion ratio and ripple are within the simulated range and do not show the effect of substrate leakage current. Yet, abnormally high input current clearly suggests the presence of substrate leakage currents.

B. Regulators

IC1 and IC2 regulators have been fully characterized. Table III summarizes and compares results for both designs. In general, measurements are in good agreement with postlayout simulations. The IC1 regulator has the advantage of operating at input voltages as high as 50 V with less than 112 μA. The IC2 regulator can be set to four different output voltages thanks to an integrated resistive ladder. If process variations prove to be unacceptable, on-chip resistor trimming may be considered but remains costly.

For the proposed neurostimulator prototype, an off-chip resistive divider can also be used for easy external voltage adjustment. For around 10-V output voltage, the IC2 regulator is clearly better in terms of drop-out voltage and load regulation.

TABLE III
HV REGULATORS POSTLAYOUT SIMULATION (SIM.) AND 10 SAMPLES MEASUREMENT RESULTS (MEAS.)

			IC2 Regulator		IC1 Regulator		
Parameter	**Conditions**	**Setup**	**Sim.**	**Meas.**	**Sim.**	**Meas.**	**Units**
Output voltage	Vin= 13V Iout= 1mA	12V	12.537	12.287 ±72m			V
		10V	10.448	10.222 ±61m	10.287	9.487 ±185m	
		5V	5.224	5.116 ±36m			
		3.3V	3.448	3.396 ±22m			
Dropout voltage	Iout= 5mA	12V	138	112			mV
		10V	141	132	437	440	
		5V	291	293			
		3.3V	738	901			
Line regulation	Vout+1V to Vmax	12V	24	48			
		10V	16	30	19	40 ±25	
		5V	7	<10			
		3.3V	5	<10			
Load regulation	1mA to 10mA	12V	44	18			
		10V	32	14	46	52	
		5V	15	<10			
		3.3V	12	<10			
Ripple rejection @100Hz	Vin= 19V +1Vpeak ripple	12V	69	73			dB
		10V	70	74	77	70 ±9	
		5V	77	75			
		3.3V	81	76			
Ripple rejection @1kHz		12V	69	52			
		10V	70	53	64	65 ±4	
		5V	77	53			
		3.3V	81	54			
GND current	Ladder	Vin= Vmax	48	33	2	<2	uA
	Reference		14	22	31	26	
	Total		153	161	141	98 ±14	
Silicon area	Reference		0.154		0.217		mm²
	Total		0.718		1		
Vin= Vout+1V; Iout= 10mA; Cout= 1uF unless otherwise stated							
Vmax= 20V or 50V for IC2 or IC1 respectively							

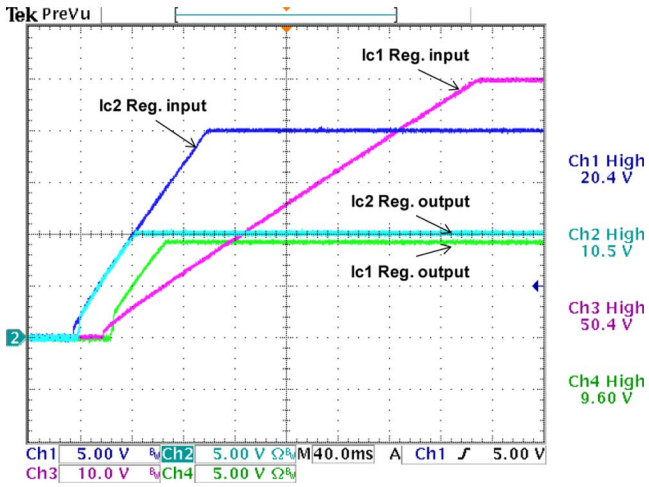

Fig. 15. Oscilloscope capture of the HV regulators startup with a maximum input voltage step.

This is mainly because its pass transistor can be driven by a Vgs as large as the supply (up to 20 V), leading to a smaller Ron even if the pass transistor silicon area is smaller. On the other hand, the IC2 regulator has a degraded ripple rejection at 1 kHz compared to simulation. This is due to the test fixture. The regulator biasing and reference signals suffer from some crosstalk with the supply as they are connected externally from the voltage reference to the regulator. Fig. 15 is an oscilloscope capture that shows IC2 and IC1 regulators' outputs (Ch2 and Ch4, respectively) in response to the input (Ch1 and Ch3, respectively) at power-on with the 20- and 50-V step, respectively. Both regulators show good stability in the presence of large input voltage variations.

C. Data Recovery

The Manchester decoder is fully functional and the clock duty cycle can be easily adjusted with a tuning voltage which can be derived from the regulator output using an external resistive divider. However, the OOK demodulator is not functional in any of the tested chips. With a limited number of I/Os, no internal node is available for investigation. Considering the substrate leakage current and latch-up issues observed in the rectifiers, the LDMOS transistor (N1, N2 in Fig. 5; N3 in Fig. 6(c); N11, N12, N21, N22 in Fig. 7) is suspected of not being suitable in those designs. This LDMOS transistor has been chosen mainly for its lower Ron and relatively smaller area, but its model was considered preliminary in the C08E design kit when we used it. This is being investigated and eventually it should be replaced by a more conventional but reliable bidirectional NMOS with double extended channels in all designs.

IV. CONCLUSION

We proposed using HV CMOS technology to fully integrate the inductive power and data-recovery front end while adopting a step-down approach where the inductive voltage is left free up to a much higher voltage (20 or 50 V). We reported the design of two consecutive HV custom ICs: IC1 and IC2, fabricated in DALSA semiconductor C08G and C08E technologies, respectively, with a total silicon area (including pads) of 4 and 9 mm^2, respectively. Both ICs include HV rectification and regulation. IC2 includes two enhanced rectifier designs, a voltage-doubler, a bridge rectifier, as well as data recovery. Successful measurement results show that HV regulators can provide a stable 3.3- to 12-V supply from an unregulated input which can be as high as 20 or 50 V for IC2 and IC1, respectively, with performance that matches simulation results. Postlayout simulations show that both rectifier designs integrated in IC2 achieve more than 90% power efficiency at a 1-mA load and provide enough room for 12-V voltage regulation at a 3-mA load and a maximum-available inductive power of 50 mW only. Unfortunately, even if the design was focusing on protecting rectifiers from substrate leakage current and latch-up, both IC2 rectifiers showed high input current draw and latch-up for higher load currents and higher input voltages. However, this may be explained by a specific LDMOS transistor that was used in IC2 rectifiers and the data demodulator while its model was considered preliminary. This is being investigated and we suggest replacing the LDMOS transistor by a bidirectional NMOS with double extended channels in the proposed designs.

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